CBCS (R19)

CURRICULUM

M. TECH. TWO YEAR PG PROGRAMME

(Applicable for the batches admitted from 2019-20)

SWARNANDHRA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
Seetharampuram, Narsapur – 534 280, W.G.Dt. Andhra Pradesh

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Andhra Pradesh

1. INTRODUCTION

Swarnandhra College of Engineering & Technology (Subsequently referred to as SCET) will be followed the norms of Jawaharlal Nehru Technological University Kakinada and Govt. of Andhra Pradesh.

Academic Programmes of the institute are governed by rules and regulations approved by the Academic Council, which is the highest Academic body of the Institute. These rules and regulations are applicable for the students of M. Tech (Regular) Course from the Academic Year 2019-20 onwards.

2. ADMISSIONS:

2.1. Admission into first year of M. Tech Programme: Admissions in each M.Tech program in the Institution are classified into **CATEGORY - A** through convener, PGECET and **GATE. CATEGORY-B** seats are filled by the college management.

2.2. Admissions with advance standing: These may arise in the following cases:

a) When a student seeks transfer from other colleges to SCET and desirous to pursue the study at SCET in an eligible branch of study.

b) When students of SCET get transferred from one regulation to another regulation or from previous syllabus to revised syllabus.

c) When a student after long discontinuity rejoins the college to complete his/her Program of study for the award of degree.

In all such cases for admission, when needed, permissions from the statutory bodies are to be obtained and the Programme of study at SCET will be governed by the transitory regulations.

3. DURATION OF THE PROGRAMME AND MEDIUM OF INSTRUCTION:

The duration of the M. Tech. Program is two academic years consisting of four semesters. Students, who fail to fulfill all the academic requirements for the award of the degree within minimum of four academic years, will forfeit their admission in M. Tech course**.** The medium of instruction and examinations are in English.

4. PROGRAMMES OF STUDY:

The following specializations are offered at present.

i) M. Tech – Power Electronics

ii) M. Tech – CAD/CAM

iii) M. Tech – VLSI System Design

iv) M. Tech – Computer Science & Engineering

v) M. Tech – Nanotechnology

vi) M. Tech – Structural Engineering

5. AWARD OF M. TECH DEGREE

- The candidate pursues a course of study in not less than two and not more than four academic years.
- The student shall register for all 68 credits and secure the same.

6. ATTENDANCE

The minimum instruction days in each semester are 90.

i. A student will be eligible to appear for end semester examinations, if he/she acquired a minimum of 75% of attendance in aggregate of all the courses.

ii. Condonation of shortage of attendance in aggregate up to 10% on medical grounds (Above 65% and below 75%) in any semester may be granted by the College Academic Committee.

iii. Shortage of Attendance below 65% in aggregate shall not be condoned

iv. Students with less than 65% of attendance in any semester are not eligible to take up their end examination of that particular semester and their registration for examination shall be allowed.

v. Attendance may also be condoned for those who participate in Intercollegiate/university sports, co- and extracurricular activities provided their attendance is in the minimum prescribed range for the purpose (>65%) and recommended by the concerned authority. He/ She shall pay the prescribed condonation fee.

vi. Prescribed Condonation fee shall be payable by the student to appear for the end examination.

vii. A Student will not be promoted to the next semester unless he/she satisfies the attendance requirement of the present semester as applicable. They may seek re-admission for that semester as and when offered consecutively by the Department.

7. EVALUATION

- The performance of the candidate in each semester shall be evaluated course-wise, with a maximum of 100 marks for both theory and practical, on the basis of Internal Evaluation and End Semester Examination.
- For the theory subjects 70 marks shall be awarded based on the performance in the End Semester Examination and 30 marks shall be awarded based on the Internal Evaluation. Internal Evaluation shall be made based on the Weighted Average of the marks secured in the two Mid Examinations conducted, one in the middle of the Semester and the other immediately after

the completion of instruction. The weightages are 80% for the mid in which the student secured highest marks and 20% for the mid in which the student secured lowest marks.

- Each mid examination shall be conducted for a total duration of 90 minutes with 3 questions from two and half units (without choice) and each question for 10 marks.
- End semester examination is conducted for 70 marks. Question paper consists of five questions from five units with internal choice. Duration of exam is 180 minutes.
- For practical courses, 30 marks for Internal Evaluation and 70 marks for external examination. Out of 30 Internal marks 15 marks shall be awarded for day-to-day work including Record work and the remaining 15 marks to be awarded by conducting internal laboratory test.
- For MOOCs Course, the student shall register for the course (Minimum of 12 weeks) offered by SWAYAM/NPTEL/JNTUK MOOCs through online with the approval of committee comprises of Head of the Department and two senior faculty. The Head of the Department shall appoint one mentor for each of the MOOC courses offered. The student needs to earn a certificate by passing the exam. The student will be awarded the credits given in curriculum only by submission of the certificate.
- A candidate shall be deemed to have secured the minimum academic requirement in a course if he secures a minimum of 40% of marks in the End semester Examination and a minimum aggregate of 50% of the total marks in the end semester Examination and Internal.
- A candidate shall be given one chance to re-register for each course provided the internal marks secured by a candidate are less than 50% and has failed in the end examination after completion of the third semester. The candidate's attendance in the re- registered course(s) shall be calculated separately to decide upon his/her eligibility for writing the end examination in those courses(s). In the event of the student taking another chance, his internal marks and end examination marks obtained in the previous attempt stand cancelled. For re-registration the candidates have to apply to the Institute by paying the requisite fees and get approval from the concern authorities before the start of the semester in which re-registration is required. In case the candidate secures less than the required attendance in any re-registered course(s), he/she shall not be permitted to write the End Examination in that course.
- Laboratory external examination must be conducted with internal and external examiner. External examiner will be appointed by the COE from the approved panel of examiners.
- The candidate has to register for the audit course mandatorily and he has to pass the audit courses for successful completion of the degree.
- For Mini Project with Seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Project Review Committee consisting of Head of the Department, supervisor/mentor and two other senior faculty members of the department. For Mini

Project with Seminar, there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

8. EVALUATION OF PROJECT/DISSERTATION WORK

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

i. A Project Review Committee (PRC) shall be constituted with Head of the Department and two other senior faculty members in the department.

ii. Registration of Dissertation/Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects, both theory and practical.

iii. After satisfying (ii), a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work for approval. The student can initiate the Project work, only after obtaining the approval from the Project Review Committee (PRC).

iv. If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the Project Review Committee (PRC). However, the PRC shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

v. Continuous assessment of Dissertation-I and Dissertation-II during the Semester(s) will be monitored by the PRC.

vi. A candidate shall submit his status report in two stages to the PRC, at least with a gap of 3 months between them.

vii. The work on the project shall be initiated at the beginning of the 3rd Semester and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of theory and practical course with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. The candidate has to pass all the theory and practical subjects before submission of the Thesis.

viii. Three copies of the Project Thesis certified by the supervisor shall be submitted to the College.

ix. The thesis shall be adjudicated by one examiner from the approved panel of examiners, by the COE.

x. Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the Thesis. The Head of the Department shall coordinate and make arrangements for the conduct of Viva-Voce examination. The Board shall jointly report the candidate's work as one of the following:

A. Excellent

B. Good

C. Satisfactory

D. Unsatisfactory

If the report of the Viva-Voce is unsatisfactory, the candidate shall retake the Viva-Voce examination only after three months. If he fails to get a satisfactory report at the second Viva-Voce examination, the candidate has to re-register for the project and complete the project within the stipulated time after taking the approval from the Concern authorities.

9. GRADING SYSTEM:

9.1 Award of Grade:

(i) Grade Point Average (GPA):

a) The Grade Point Average (GPA) will be calculated according to the formula.

$$GPA = \frac{\sum C_i G_i}{\sum C_i}$$

Where C_i = number of credits for the subject i

G_i = grade points obtained by the student in the subject.

b) Semester Grade Point Average (SGPA) is awarded to candidates considering all the subjects of the semester. Zero grade points are also included in this computation.

c) To arrive at Cumulative Grade Point Average (CGPA), the formula is used considering the student's performance in all the courses taken in all the semesters completed up to the particular point of time.

$$CGPA = \frac{\sum C_i G_i}{\sum C_i}$$

Where C_i = number of credits for the subject i

G_i = grade points obtained by the student in the subject.

(ii) After a student satisfies the requirements prescribed for the award of M. Tech Program he/she shall be placed in one of the following four grades. The award of the degree is based on CGPA on a grade point scale of 10.

CGPA	Award of Division
≥7.75	First Class with Distinction
≥6.75	First Division
≥5.75	Second Division
<5.75	Unsatisfactory

9.2 Award of Grade in Each Semester:

a. Based on the performance during a given semester, a final letter grade will be awarded at the end of the semester for each subject. The letter grades and the corresponding grade points are as given in the Table.

Percentage of Marks Scored	Letter Grade	Level	Grade points
>=90	O	Outstanding	10
80– 89	S	Excellent	9
70-79	A	Very Good	8
60-69	B	Good	7
50-59	C	Fair	6
< 50	F	Fail	0
		Absent	0

b. Grade Sheet: A grade sheet (memorandum) will be issued to each student indicating his performance in all courses taken in that semester and also indicating the Grades.

c. Transcripts: After successful completion of the total program of study, a Transcript containing performance of all academic years will be issued as a final record. Duplicate transcripts will also be issued up to any point of study to any student on request and by paying the stipulated fee in force.

d. Candidates shall be permitted to apply for revaluation within the stipulated period with payment of prescribed fee.

10. CONDUCT AND DISCIPLINE:

Students admitted in SCET are to be followed the conduct and discipline of the college and which will be updated from time to time.

11. MALPRACTICES:

If any malpractices held in internal assessment tests or Semester-End Examinations, Principal constitute a Malpractice Enquiry Committee to enquire the case. The principal shall take necessary action based on the recommendations of the committee as per stipulated norms.

12. <u>WITHHOLDING OF RESULTS</u>

If the student has not paid the dues, if any, to the university or if any case of indiscipline is pending against him, the result of the student will be withheld. His degree will be withheld in such cases.

13. <u>GENERAL</u>

- Wherever the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”, “hers”.
- The academic regulation should be read as a whole for the purpose of any interpretation.

- In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Chairman, Academic Council is final.
- The College may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the College.

I-SEMESTER

S.No	Course Code	Course Title	L	T	P	C	IM	EM	TM
1	19VL1T01	Digital Design using HDL	3	-	-	3	30	70	100
2	19VL1T02	VLSI Technology and Design	3	-	-	3	30	70	100
3	19VL1E01 19CM1E07 19CM1E08	**Elective I** **1.** Digital System Design 2. Advanced Operating Systems 3 Soft Computing Techniques	3	-	-	3	30	70	100
4	19VL1E04 19CM1E09 19VL1E06	**Elective II** **1.** CPLD and FPGA Architecture and Applications 2. Advanced Computer Architecture 3. VLSI Signal Processing	3	-	-	3	30	70	100
5	19VL1L01	Digital Design using VHDL Laboratory		-	4	2	30	70	100
6	19VL1L02	MOS Layout design Laboratory		-	4	2	30	70	100
7	19CC1T01	Research methodology and IPR	2	-		2	30	70	100
8		Audit Course I	2	-	-	0	-	-	-
		TOTAL				18			

II -SEMESTER

S.No	Course Code	Course Title	L	T	P	C	IM	EM	TM
1	19VL2T01	Analog and Digital CMOS VLSI Design	3	-	-	3	30	70	100
2	19VL2T02	Low Power VLSI Design	3	-	-	3	30	70	100
3	19VL2E07 19VL2E08 19VL2E09	**Elective III** **1.** Hardware Software Co-Design 2. CAD for VLSI 3. DSP Processors & Architectures	3	-	-	3	30	70	100
4	19VL2E10 19VL2E11 19VL2E12	**Elective IV** **1.** Semiconductor Memory Design and Testing 2.NANO Technology and applications 3. System on Chip Design	3	-	-	3	30	70	100
5	19VL2L01	Digital Design using Verilog HDL Laboratory		-	4	2	30	70	100
6	19VL2L02	VLSI Design and verification Laboratory		-	4	2	30	70	100
7	19VL2P01	Mini Project (Seminar)	-	-	4	2	50	-	50
8		Audit Course II	2	-	-	0	-	-	-
		TOTAL				18			

III-SEMESTER

S. No.	Course Code	Course Title	L	T	P	C	IM	EM	TM
1	19VL3E13 19VL3E14 19VL3E15	**Programme specific elective** 1. Embedded System Design 2. Design For Testability 3.CMOS Mixed Signals Circuit Design	3	-	-	3	30	70	100
2	19CM3O01 19CC3O02 19CC3O03 19MB3O04 19CC3O05 19PE3O06	**Open Elective** 1.Business Analytics 2.Industrial Safety 3.Operations Research 4.Cost Management of Engineering Projects 5.Composite Materials 6.Waste to Energy	3	-	-	3	30	70	100
3		Dissertation Phase I/ Industrial Project			20	10	-	-	-
		TOTAL				16			

IV- SEMESTER

S. No.	Course Code	Course Title	L	T	P	C	IM	EM	TM
1	19VL4P01	Dissertation Phase II/ Project	-	-	32	16	-	-	-
		TOTAL				16			

Audit course I & II

S.No	Course Code	Course Title
1	19ACXM01	English for Research Paper Writing
2	19ACXM02	Disaster Management
3	19ACXM03	Sanskrit for Technical Knowledge
4	19ACXM04	Value Education
5	19ACXM05	Constitution of India
6	19ACXM06	Pedagogy Studies
7	19ACXM07	Stress Management by Yoga
8	19ACXM08	Personality Development through Life Enlightenment skills

- 'X' indicates semester number

M.Tech 1st SEMESTER	L	P	C
	4	0	3
DIGITAL DESIGN USING HDL			

UNIT-I:
Digital Logic Design using VHDL

Introduction, designing with VHDL, design entry methods, logic synthesis , entities , architecture , packages and configurations, types of models: dataflow , behavioral , structural, signals vs. variables, generics, data types, concurrent vs. sequential statements , loops and program controls.

Digital Logic Design using Verilog HDL
Introduction, Verilog Data types and Operators, Binary data manipulation, Combinational and Sequential logic design, Structural Models of Combinational Logic, Logic Simulation, Design Verification and Test Methodology, Propagation Delay, Truth Table models using Verilog.

UNIT-II:
Combinational Logic Circuit Design using VHDL
Combinational circuits building blocks: Multiplexers, Decoders , Encoders , Code converters, Arithmetic comparison circuits , VHDL for combinational circuits , Adders-Half Adder, Full Adder, Ripple-Carry Adder, Carry Look-Ahead Adder, Subtraction, Multiplication.
Sequential Logic Circuit Design using VHDL
Flip-flops, registers & counters, synchronous sequential circuits: Basic design steps, Mealy State model, Design of FSM using CAD tools, Serial Adder Example, State Minimization, Design of Counter using sequential Circuit approach.

UNIT-III: Digital Logic Circuit Design Examples using Verilog HDL
Behavioralmodeling , Data types, Boolean-Equation-Based behavioral models of combinational logics , Propagation delay and continuous assignments , latches and level-sensitive circuits in Verilog, Cyclic behavioral models of flip-flops and latches and Edge detection, comparison of styles for behavioral model; Behavioral model, Multiplexers, Encoders and Decoders, Counters, Shift Registers, Register files, Dataflow models of a linear feedback shift register, Machines with multi cycle operations, ASM and ASMD charts for behavioralmodeling, Design examples, Keypad scanner and encoder.

UNIT-IV: Synthesis of Digital Logic Circuit Design
Introduction to Synthesis, Synthesis of combinational logic, Synthesis of sequential logic with latches and flip-flops, Synthesis of Explicit and Implicit State Machines, Registers and counters.

UNIT-V: Testing of Digital Logic Circuits and CAD Tools
Testing of logic circuits, fault model, complexity of a test set, path-sensitization, circuits with tree structure, random tests, testing of sequential circuits, built in self test, printed circuit boards, computer aided design tools, synthesis, physical design.

TEXT BOOKS:
1. Stephen Brown &ZvonkoVranesic, ”Fundamentals of Digital logic design with VHDL”, Tata McGraw Hill,2nd edition.
2. Michael D. Ciletti, “Advanced digital design with the Verilog HDL”, Eastern economy edition, PHI.

REFERENCE BOOKS:
1. Stephen Brown &ZvonkoVranesic, ”Fundamentals of Digital logic with Verilog design”, Tata McGraw Hill,2nd edition.
2. Bhaskar, ”VHDL Primer”,3rd Edition, PHI Publications.
3. Ian Grout, “Digital systems design with FPGAs and CPLDs”, Elsevier Publications.

M.Tech 1st SEMESTER	L	P	C
	4	0	3
VLSI TECHNOLOGY AND DESIGN			

UNIT-I:

VLSI Technology: Fundamentals and applications, IC production process, semiconductor processes, design rules and process parameters, layout techniques and process parameters.
VLSI Design: Electronic design automation concept, ASIC and FPGA design flows, SOCdesigns, design technologies: combinational design techniques, sequential design techniques, state machine logic design techniques and design issues.

UNIT-II:
CMOS VLSI Design: MOS Technology and fabrication process of pMOS, nMOS, CMOS andBiCMOS technologies**,** comparison of different processes.
Building Blocks of a VLSI circuit: Computer architecture, memory architectures,communication interfaces, mixed signal interfaces.
VLSI Design Issues: Design process, design for testability, technology options, powercalculations, package selection, clock mechanisms, mixed signal design.

UNIT-III:
Basic electrical properties of MOS and BiCMOS circuits, MOS and BiCMOS circuit design processes, Basic circuit concepts, scaling of MOS circuits-qualitatitive and quantitative analysis with proper illustrations and necessary derivations of expressions.

UNIT-IV:
Subsystem Design and Layout: Some architectural issues, switch logic, gate logic, examples ofstructured design (combinational logic), some clocked sequential circuits, other system considerations.
Subsystem Design Processes: Some general considerations and an illustration of designprocesses, design of an ALU subsystem.

UNIT-V:
Floor Planning: Introduction**,** Floor planning methods, off-chip connections.
Architecture Design: Introduction, Register-Transfer design, high-level synthesis, architecturesfor low power, architecture testing.
Chip Design: Introduction and design methodologies.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian, Douglas A. Pucknell, SholehEshraghian, 2005, PHI Publications.
2. Modern VLSI Design-Wayne Wolf, 3rd Ed., 1997, Pearson Education.
3. VLSI Design-Dr.K.V.K.K.Prasad, KattulaShyamala, Kogent Learning Solutions Inc., 2012.

REFERENCE BOOKS:

1. VLSI Design Technologies for Analog and Digital Circuits, Randall L.Geiger, Phillip E.Allen, Noel R.Strader, TMH Publications, 2010.
2. Introduction to VLSI Systems: A Logic, Circuit and System Perspective- Ming-BO Lin, CRC Press, 2011.
3. Principals of CMOS VLSI Design-N.H.E Weste, K. Eshraghian, 2nd Edition, Addison Wesley.

M.Tech 1st SEMESTER	L	P	C
	4	0	3
ADVANCED OPERATING SYSTEMS (ELECTIVE-I)			

UNIT-I: Introduction to Operating Systems
Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System

UNIT-II: Introduction to UNIX and LINUX
Basic Commands & Command Arguments, Standard Input, Output, Input / Output Redirection, Filters and Editors, Shells and Operations

UNIT –III:
System Calls: System calls and related file structures, Input / Output, Process creation & termination.
Inter Process Communication: Introduction, File and record locking, Client – Server example, Pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT –IV:
Introduction to Distributed Systems: Goals of distributed system, Hardware and software concepts, Design issues.
Communication in Distributed Systems: Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication.

UNIT –V:
Synchronization in Distributed Systems: Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions
Deadlocks: Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

TEXT BOOKS:
1. The Design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI.
2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.
3. The Complete Reference LINUX – Richard Peterson, 4th Ed., McGraw – Hill.

REFERENCE BOOKS:

1. Operating Systems: Internal and Design Principles - Stallings, 6th Ed., PE.
2. Modern Operating Systems - Andrew S Tanenbaum, 3rd Ed., PE.
3. Operating System Principles - Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Ed., John Wiley
4. UNIX User Guide – Ritchie & Yates.
5. UNIX Network Programming - W.Richard Stevens, 1998, PHI.

M.Tech 1st SEMESTER	L	P	C
	4	0	3
ADVANCED COMPUTER ARCHITECTURE (ELECTIVE II)			

UNIT- I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces ofcomputing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law.

Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT – II

Pipelines: Introduction ,basic RISC instruction set ,Simple implementation of RISC instruction set,Classic five stage pipe line for RISC processor, Basic performance issues in pipelining , Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducingcache miss penalty, Virtual memory.

UNIT - III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamicscheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach,Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT – IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT – V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues ininterconnecting networks, Examples of inter connection, Cluster, Designing of clusters. **Intel Architecture:** Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls

TEXT BOOK:

1. John L. Hennessy, David A. Patterson, "Computer Architecture: A Quantitative Approach", 3rd Edition, Elsevier.

REFERENCE BOOKS

1. John P. Shen and Miikko H. Lipasti, "Modern Processor Design: Fundamentals of Super Scalar Processors", 2002, Beta Edition, McGraw-Hill
2. Kai Hwang, Faye A.Brigs., "Computer Architecture and Parallel Processing", McGraw Hill.
3. DezsoSima, Terence Fountain, Peter Kacsuk , "Advanced Computer Architecture - A Design Space Approach", Pearson Education.

M.Tech 1st SEMESTER	L	P	C
	4	0	3
RESEARCH METHODOLOGY AND IPR			

UNIT-I:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT-II:

Effective literature studies approaches, analysis, Plagiarism, Research ethics

UNIT-III:

Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT-IV:

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT-V:

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc.Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

REFERENCES:

1. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
3. Mayall, "Industrial Design", McGraw Hill, 1992.
4. Niebel, "Product Design", McGraw Hill, 1974.
5. Asimov, "Introduction to Design", Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016.
7. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

M.Tech 1st SEMESTER	L	P	C
	4	0	3
DISASTER MANAGEMENT (Audit Course - I)			

UNIT-I:

Introduction:

Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude. **Disaster Prone Areas in India:**

Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics

UNIT-II:

Repercussions of Disasters and Hazards:

Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT-III:

Disaster Preparedness and Management:

Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT-IV:

Risk Assessment Disaster Risk:

Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation.Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment.Strategies for Survival.

UNIT-V:

Disaster Mitigation:

Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

TEXT BOOKS/ REFERENCES:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal book Company.
2. Sahni, PardeepEt. Al. (Eds.)," Disaster Mitigation Experiences and Reflections", Prentice Hall of India, New Delhi.
3. Goel S. L., Disaster Administration and Management Text and Case Studies", Deep &Deep Publication Pvt. Ltd., New Delhi.

SEMESTER- II	L	T	P	C
	3	-	-	3
19VL2T01 : ANALOG AND DIGITAL CMOS VLSI DESIGN				

COURSE OUTCOMES
Students will be able to

CO1. Analyze analog and digital circuits using CMOS logic.
CO2. Design the analog and digital circuits constrained by the design metrics.
CO2. Optimize and connect the individual gates to form the building blocks of a system.
CO3. Design simulation using EDA tools like Cadence, Mentor Graphics and other open source software tools like NGSPICE

Digital CMOS Design:

UNIT-I: Review:

Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models. Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their evaluation, Dynamic behavior, Power consumption.

UNIT-II Physical design flow:

Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model. Combinational logic: Static CMOS design, Logic effort, Ratioed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.

UNIT-III Sequential logic:

Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, Non-bistable sequential circuit. Advanced technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, TFET etc.

Analog CMOS Design:

UNIT-IV Single Stage Amplifier:

CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common-gate stage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

UNIT-V

Passive and active current mirrors: Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise

TEXTBOOKS:

1. J P Rabaey, A P Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall

electronics and VLSI series, 2nd Edition.

2. Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2 nd Edition.

REFERENCES:

1. BehzadRazavi , "Design of Analog CMOS Integrated Circuits", TMH, 2007.
2. Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford, 3rd Edition.
3. R J Baker, "CMOS circuit Design, Layout and Simulation", IEEE Inc., 2008.
4. Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits, Analysis and Design", TMH, 3rd Edition.
5. Pucknell, D.A. and Eshraghian, K., "Basic VLSI Design", PHI, 3rd Edition

SEMESTER-II	L	T	P	C
	3	-	-	3
19VL2T02 : LOW POWER VLSI DESIGN				

Course Outcomes: At the end of the course, students will be able to:

CO1. Identify the sources of power dissipation in digital IC systems & understandthe impact of power on system performance and reliability.

CO2. Characterize and model power consumption & understand the basic analysismethods.

CO3. Understand leakage sources and reduction techniques.

UNIT-I

Sources of power dissipation in digital ICs, emerging low power approaches, dynamic dissipation in CMOS, effects of Vdd & Vt on speed, constraints on Vt reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations.

UNIT-II

Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.Low Power Clock Distribution: Power dissipation in clock distribution.

UNIT-III

Logic Synthesis for Low Power estimation techniques: Power minimization techniques, low power arithmetic components- circuit design styles, adders, multipliers.

UNIT-IV

Low Power Memory Design: Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits.

UNIT-V

Low Power Microprocessor Design System: power management support, architectural trade offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power & performance.

TEXTBOOKS

1. P. Rashinkar, Paterson and L. Singh, "Low Power Design Methodologies", Kluwer Academic, 2002
2. Kaushik Roy, Sharat Prasad, "Low power CMOS VLSI circuit design", John Wiley sons Inc.,2000.

REFERENCES:

1. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley, 1999.
2. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer,1995
3. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.

SEMESTER-II	L	T	P	C
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19VL2E09 : DSP PROCESSORS AND ARCHITECTURES

COURSE OUTCOMES

Students are able to

CO1. Understand the basics of Digital Signal Processing and transforms.
CO2. Distinguish between the architectural features ofGeneral
purpose processors and DSP processors.
CO3. Understand the architectures of TMS320C54xx devices and ADSP 2100 DSPdevices.
CO4. Write simple assembly language programs using instruction set of TMS320C54xx andinterface various devices to DSP Processors

UNIT – I: Introduction to Digital Signal Processing: Introduction, A Digital signal- processing system, The sampling process, Discrete time sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation. **Computational Accuracy in DSP Implementations:** Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors,D/A Conversion Errors, Compensating filter.

UNIT – II: Architectures for Programmable DSP Devices: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT-III: Programmable Digital Signal Processors: Commercial digital signal processing devices, Data Addressing modes of TMS320C54XX DSps, data Addressing moes of TMS320C54XX Processors, Memory space of TMS320C54XX processors, program control, TMS320C54XX instructions and programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, pipeline Operation of TMS320C54XX Processors.

UNIT – IV: Analog Devices Family of DSP Devices: Analog Devices Family of DSP Devices- ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP- 2181 high performance processor. **Introduction to Blackfin Processor**- The Blackfin Processor, Introduction to Micro signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT – V: Interfacing Memory and I/O Peripherals to Programmable DSP Devices: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009
3. Embedded Signal Processing with the Micro Signal Architecture Publisher: Woon-Seng Gan, Sen M. Kuo, Wiley-IEEE Press, 2007

REFERENCE BOOKS:

1. Digital Signal Processors, Architecture, Programming and Applications–B. Venkataramaniand M. Bhaskar, 2002, TMH.
2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.
3. DSP Processor Fundamentals, Architectures & Features – Lapsley et al., S. Chand & Co.
4. Digital Signal Processing Applications Using the ADSP-2100 Family, Amy Mar, PHI
5. The Scientist and Engineer's Guide to Digital Signal Processing by Steven W. Smith, California Technical Publishing
6. Embedded Media Processing, David J. Katz and Rick Gentile of Analog Devices, Newnes

SEMESTER-I	L	T	P	C
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19VL2E12 SYSTEM ON CHIP DESIGN				

UNIT-I: Introduction to the System Approach

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT-II: Processors

Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT-III: Memory Design for SOC

Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT-IV: Interconnect Customization and Configuration

Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance-Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT-V: Application Studies / Case Studies

SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Computer System Design System-on-Chip – Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd
2. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer

REFERENCE BOOKS:

1. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.
2. System on Chip Verification – Methodologies and Techniques – Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

M.Tech III SEMESTER	L	P	C
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DESIGN FOR TESTABILITY			

UNIT I
INTRODUCTION TO TESTING:
Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT II
LOGIC AND FAULT SIMULATION:
Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT III
TESTABILITY MEASURES:
SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT IV
BUILT-IN SELF-TEST:
The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-PerScan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT V
BOUNDARY SCAN STANDARD:
Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXTBOOKS:

1. M.L. Bushnell, V. D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits” Kluwer Academic Publishers.

REFERENCES:

1. M. Abramovici, M. A. Breuer and A.D Friedman, “Digital Systems and Testable Design”, Jaico Publishing House.
2. P.K. Lala, “Digital Circuits Testing and Testability”, Academic Press.

M.Tech III SEMESTER	L	P	C
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WASTE TO ENERGY			

Course Outcomes: After successful completion of this course, students should be able to

CO1: Understand the principles associated with effective energy management and to apply these principles in the day to day life.

CO2: Develop insight into the collection, transfer and transport of municipal solid waste.

CO3: Analyse the design and operation of a municipal solid wasteland fill

CO4: Analyse the main operational challenges in operating thermal and biochemical energy from waste facilities.

UNIT-I
Introduction to Energy from Waste:

Introduction to Energy from Waste: Classification of waste as fuel - Agro based - Forest residue - Industrial waste – MSW - Conversion devices – Incinerators – Gasifiers – Digestors

UNIT-II
Biomass Pyrolysis

Biomass Pyrolysis: Pyrolysis – Types - Manufacture of charcoal - Methods, Yields and application - Manufacture of pyrolytic oils and gases - yields and applications.

UNIT-III
Biomass Gasification

Gasifiers - Fixed bed system - Downdraft and updraft gasifiers - Fluidized bed gasifiers - Design, construction and operation - Gasifier burner arrangement for thermal heating - Gasifier engine arrangement and electrical power - Equilibrium and kinetic consideration in gasifier operation.

UNIT-IV
Biomass Combustion

Biomass stoves - Improved chullahs – types - some exotic designs - Fixed bed combustors – Types - Inclined grate combustors - Fluidized bed combustors - Design, construction and operation - Operation of all the above biomass combustors.

UNIT-V
Biogas

Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction = biochemical conversion - anaerobic digestion -Bio diesel production = Biomass energy programme in India.

Text Books:

1. Desai, Ashok V, “Non Conventional Energy”, Wiley Eastern Ltd., 1990.

Reference Books:

1. Khandelwal, K. C. and Mahdi, S. S, “Biogas Technology - A Practical Hand Book”, Vol. I & II Tata McGraw Hill Publishing Co. Ltd., 1983.
2. Challal, D. S, “Food, Feed and Fuel from Biomass”, IBH Publishing Co. Pvt. Ltd., 1991.